CLAIMS:

1. A bus system for use with an information processing apparatus comprising:

a processor bus connected to at least a processor;

a memory bus connected to a main memory;

a system bus connected to at least a connected device;

connection controller connected to control buses and address buses respectively of said processor bus, said memory bus, and said system bus for generating a data path control signal and for producing a control signal and an address signal for at least either one of said processor bus, said memory bus, and said system bus; and

data switch means connected to data buses respectively of said processor bus, said memory bus, and said system bus for directly transferring, in response to the data path control signal from said connection controller, data from either one of said data buses to another one thereof.

2. A bus system according to Claim 1 wherein said data switch means comprises:

latch means for respectively storing therein the data from said data buses respectively of said processor bus, said memory bus, and said system bus;

first select means disposed respectively in association with said processor bus, said memory bus,

and said system bus, each said first select means selecting outputs from two said latch means other than said latch means related thereto; and

first generate means for receiving as an input thereto the data path control signal and for generating, in response to the data path control signal, a select signal of said first select means.

3. A bus system according to Claim 1 wherein said connection controller comprises:

second select means for respectively selecting address signals transmitted via said address buses respectively of said processor bus and said system bus, the selected address signals being sent to said address bus of said memory bus; and

second generate means for receiving as inputs thereto control signals and the address signals respectively transmitted via said control bus and said address bus respectively of said processor bus and said system bus and for generating at least the data path control signal, the select signal of said second select means, and the control signal to be delivered to said control bus of said memory bus.

4. A bus system according to Claim 1 wherein said processor bus is connected to at least a cache memory system.

5. A bus system according to Claim 1 wherein the processor connected to said processor bus is connected to a cache memory system.

6. A bus system according to Claim 1 wherein said processor bus, said memory bus, and said system bus each are of an address/data separation type.

7. A bus system according to Claim 1 wherein said processor bus, said memory bus, and said system bus each are of an address/data multiplexed type.

8. A bus system for use with an information processing apparatus including at least processors, a main memory, and input/output devices comprising:

a processor bus connected to at least one said processor;

a memory bus connected to said main memory;

a system bus connected to at least one said input/output device;

a connection controller connected to control buses and address buses respectively of said processor bus, said memory bus, and said system bus for producing a data path control signal for a change of a data path on said data buses and for generating a control signal and an address signal to at least either one of said processor bus, said memory bus, and said system bus; and

data switch means connected to data buses respectively of said processor bus, said memory bus, and said system bus for transferring, in response to the data path control signal from said connection controller, the data from either one of said data buses to another one of said data buses.

9. A bus system according to Claim 8 wherein said data switch means comprises:

latch means for respectively storing therein the data from said data buses respectively of said processor bus, said memory bus, and said system bus;

first select means disposed respectively in association with said processor bus, said memory bus, and said system bus, each said first select means selecting outputs from two said latch means other than said latch means related thereto; and

first generate means for receiving as an input thereto the data path control signal and for generating, in response to the data path control signal, a select signal of said first select means.

10. A bus system according to Claim 8 wherein said connection controller comprises:

second select means for respectively selecting address signals transmitted via said address buses respectively of said processor bus and said system bus, the selected address signals being sent to said address bus of said memory bus; and

second generate means for receiving as inputs thereto at least control signals respectively transmitted via said control bus and said address bus respectively of said processor bus and said system bus and for generating the data path control signal and the select signal of said second select means.

11. A bus system according to Claim 8 wherein

said connection controller initiates a cooperative operation of said processor bus and said memory bus in response to the data path control signal.

12. A bus system according to Claim 8 wherein said connection controller activates a cooperative operation of said system bus and said memory bus in response to the data path control signal.

13. A bus system for use with an information processing apparatus including processors, a main memory, and input/output devices comprising:

a processor bus connected to at least one said processor;

a memory bus connected to said main memory;

a system bus connected to at least one said input/output device; and

connection control means respectively connected to said processor bus, said memory bus, and said system bus for producing a data path control signal for a change of a data path on said data buses respectively connected to said processor bus, said memory bus, and said system bus in response to control signals and address signals transmitted via said processor bus and said system bus and for transferring, in response to the data path control signal, the data from either one of said data buses to another one of said data buses.

14. A bus system according to Claim 13 wherein said connection control means includes data switch means connected to data buses respectively of said

processor bus, said memory bus, and said system bus for transferring, in response to the data path control signal, the data from either one of said data buses to another one of said data buses.

15. A bus system according to Claim 14 wherein said connection control means comprises select means for selecting the address signals respectively from said processor bus and said system bus, the selected address signals being sent to said address bus of said memory bus.

16. A bus system according to Claim 15 wherein said connection control means includes generate means for receiving as inputs thereto the control signals and the address signals from said processor bus and said system bus for generating the data path control signal and a select signal of said select means.

17. A bus system according to Claim 13 wherein said processor bus is connected to at least a cache memory system.

18. A bus system according to Claim 13 wherein said processor connected to said processor bus is connected to a cache memory system.

19. A bus system according to Claim 13 wherein said processor bus, said memory bus, and said system bus each are of an address/data separation type.

20. A bus system according to Claim 13 wherein said connection control means is connected to a second processor bus other than said processor bus, said second processor bus being connected to at least a processor.